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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,720	12/16/2003	Tokio Miyasita	030712-20	3461

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EXAMINER	
JACKSON, BLANE J	

ART UNIT	PAPER NUMBER
2618	

DATE MAILED: 09/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/735,720	MIYASITA ET AL.	
	Examiner	Art Unit	
	Blane J. Jackson	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Claims 5-33 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 19 June 2006.

Priority

Receipt is acknowledged of papers submitted under 35 U.S. C. 119(1)-(d), which papers have been placed of record in the file.

Specification

The title of the invention is not descriptive. In view of the elected group of claims per the Restriction, a new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

The claims are objected to because they include reference characters, which are not enclosed within parentheses.

Reference characters corresponding to elements recited in the detailed description of the drawings and used in conjunction with the recitation of the same element or group of elements in the claims should be enclosed within parentheses so

as to avoid confusion with other numbers or characters which may appear in the claims. See MPEP § 608.01(m).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leifso et al. (US 6,870,425) in view of Si (US 6,894,563).

As to claim 1, Leifso teaches a variable gain amplifier comprising:

a differential input amplifier which includes transistors T1 and T2 that constitutes a differential pair (figure 2, column 5, lines 6-27. differential amplifier (102), transistors (108) and (110)),

a constant current circuit that operates as an absorption current circuit for the transistors T1 and T2 constituting the differential pair (figure 2, column 5, lines 29-33, transistor (116) to current source the transistors to ground),

a variable impedance connected between *emitters* of the respective transistors T1 and T2 of said differential input amplifier (figure 2, column 5, lines 19-29, degeneration transistors (112) and (114) with DCTRL signal to variably control the degeneration resistance and current of the amplifier),

Wherein a gain of said differential input amplifier is made variable by variably controlling a value of said variable impedance (figure 2, column 4, line 55 to column 5, line 5).

Note: Leifso also teaches automatic load control as a parallel means to control the gain of the amplifier, column 5, lines 19-23.

Leifso teaches the variable impedance is connected between *the emitters of the respective bipolar transistors T1 and T2* but does not teach the variable impedance is connected between the *sources* of the respective transistors where "sources" indicates transistors T1 and T2 are FET's.

Si teaches automatic gain control of a differential amplifier also using variable degeneration resistance, figure 2. Si discloses the variable resistance of degeneration transistors (M8) and (M9) are field effect transistors connected between the current source (M5) or ((M10) and the respective amplifier pair transistors (M6) and (M7), column 3, lines 38 to column 4, line 10.

Since Si teaches the automatic variable resistance degeneration circuit may be applied to a voltage to current (bipolar transistor) input differential pair or a voltage to voltage (FET) input differential pair, column 1, line 66 to column 2, line 39, it would have been obvious to one of ordinary skill in the art at the time of the invention to realize the bipolar transistors and associated biasing in the input differential amplifier pair of Leifso may be exchanged for a field effect transistor pair as taught by Si to have voltage to voltage rather than a transconductance type gain topology.

As to claim 2, Leifso of Leifso modified teaches a variable gain amplifier according to claim 1 wherein said transistors T1 and T2 constituting said differential pair have their gates respectively connected to differential inputs and have their drains respectively connected to ends of load resistances being respectively connected to a supply voltage VDD at their other ends (figures 1, 2 and 5, column 8, lines 16-41, differential amplifier (149) illustrates load resistors (152) and (154) connected between the voltage supply VDD and the differential pair),

Drain-source paths of transistors T3 and T4 which serve as said variable impedance are respectively inserted and connected between the sources of said respective transistors T1 and T2 and the constant current circuit (figure 2, column 5, lines 23-31, degeneration FET transistors (112) and (114) coupled between the differential pair and the constant current circuit (116)),

A gain control voltage is connected to gates of the transistors T3 and T4 (figure 2, column 5, lines 27-29, voltage control signal DCTRL),

Whereby the gain of said differential input amplifier is variably controlled by controlling the value of said variable impedance (column 4, line 55 to column 5, line 5).

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leifso et al. (US 6,870,425) and Si (US 6,894,563) in view of Shkap (US 6,414,547).

As to claim 3, Leifso of Leifso modified teaches a variable gain amplifier according to claim 1 wherein said transistors T1 and T2 constituting said differential pair have their gates respectively connected to differential inputs and have their drains

respectively connected to ends of load resistances being respectively connected to a supply voltage VDD at their other ends (figures 1, 2 and 5, column 8, lines 16-41, differential amplifier (149) illustrates load resistors (152) and (154) connected between the voltage supply VDD and the differential pair),

Drain-source paths of transistors T3 and T4 which serve as said variable impedance are respectively inserted and connected between the sources of said respective transistors T1 and T2 (figure 2, column 5, lines 23-31, degeneration FET transistors (112) and (114) coupled between the differential pair and the constant current circuit (116)),

A gain control voltage is connected to gates of the transistors T3 and T4 (figure 2, column 5, lines 27-29, voltage control signal DCTRL),

Whereby the gain of said differential input amplifier is variably controlled by controlling the value of said variable impedance (column 4, line 55 to column 5, line 5).

Leifso modified teaches a constant current circuit (figure 2, (116)) but does not teach wherein the constant current circuit includes a first constant current circuit and a second constant circuit.

Shkap teaches a differential variable gain amplifier comprising a differential transistor input circuit (19 and 20), variable degeneration transistors (3, 4 and 5) to control the gain of the amplifier and a first and second constant current circuit, figure 1, column 1, line 66 to column 2, line 64. Shkap discloses the first and second constant current source is provided by inductors (13 and 14) that couple respectively the source of a transistor of the input differential pair to the ground terminal (21), each inductance

appearing as a high impedance path at the RF operating frequency and a short circuit to ground potential terminal for direct current, column 2, lines 13-21.

Since Shkap teaches a variable gain amplifier that is functionally equivalent to Leifso modified, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the configuration of the current source of Leifso modified in the topology of Shkap for independent biasing of the transistor input circuit direct to ground.

As to claim 4, Leifso modified teaches the variable gain amplifier according to claim 2 but does not teach the variable gain amplifier further comprising a resistance which determines a minimum gain of said differential input amplifier and which is connected between said sources of said transistors T1 and T2.

Shkap teaches a variable gain differential amplifier including a gain control device comprising variable degeneration transistors (3, 4 and 5) and a resistive circuit including capacitor (9), resistor (11), resistor (12) and capacitor (12) which is connected in parallel to the degeneration transistors. Shkap indicates the gain control device is connected between the sources (emitters) of the input amplifier transistors and functions as a variable resistance which effectively degenerates the input differential pair, column 2, lines 22-53. It is concluded the resistive circuit of Shkap determines a minimum gain of the differential input amplifier evident when the degeneration resistors are biased/controlled off, essentially isolated the sources of the transistors of the input amplifier pair at the operational frequency, column 3, lines 54-65.

It would have been obvious to one of ordinary skill in the art at the time of the invention to recognize the gain control circuits of Leifso modified would benefit from the parallel resistive circuit in the gain control device of Shkap to define the minimum gain of the variable gain amplifier.

Conclusion

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes: Harford (US 4,344,044), Harford (US 4,378,528), Lunn (US 3,641,450), Betti et al. (US 5418,494), Jones (US 3,840,756), Harford (US 4,345,214) and Imbornone et al. (US 6,342,813).

Of particular interest but predated by the applicant's effective filing date is Caresosa et al. (US 7,034,606) which essentially teaches all the claimed subject matter as shown in figure 9.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.